	Application No.	Applicant(s)
Notice of Allowability	09/594,205	HUIE ET AL.
	Examiner	Art Unit	
	Michael S. A. Delgado	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--
All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to _10/03/2005_.

2. ☒ The allowed claim(s) is/are _1-11_.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some*   c) ☐ None of the:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

    * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .

    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of

        Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☒ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)

3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____

4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application (PTO-152)

6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .

7. ☒ Examiner's Amendment/Comment

8. ☒ Examiner's Statement of Reasons for Allowance

9. ☐ Other _____ .

DAVID WILEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

1.   An examiner's amendment to the record appears below. Should the changes and/or

additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the

payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with

Michael L. Gencarella on 12/20/05.

The application has been amended as follows:

1.   (Currently Amended) A high performance network address processor comprising:

a longest prefix match lookup table for receiving a network address request having a

designated network destination address, the longest prefix match lookup table having multiple

pipelined lookup tables, a first pipelined lookup table having a single row of a first set of data

pairs, the first set of data pairs including a key value and a mask value, the mask value indicating

a number of least significant bits that are ignored within the key value, the first set of pairs being

ordered according to corresponding mask values, a second pipelined lookup table having a

plurality of rows of a second set of data pairs, the second set of data pairs including a key value

and a mask value, the mask value of the second set indicating a number of least significant bits

that are ignored within the key value; and

an associated data engine coupled to the longest prefix match lookup table that is capable

of receiving a key and an output address pointer from the longest prefix match lookup table and

that is capable of providing a network address processor data output corresponding to the

designated network address pointer.

2.   (Currently amended) The high performance network address processor of claim 1

wherein the longest prefix match lookup engine <u>includes</u> a third pipelined lookup table having a

plurality of rows of a third set of data ~~pairs~~ tuples, <u>the data tuples including a key value, a mask</u>

<u>value and a pointer value</u>.

3.   (Previously presented) The high performance network address processor of claim 1

wherein a value representing a position of a selected element in the single row of a first set of

data pairs is an input to the second pipelined lookup table, the input used to select one of the

plurality of rows of the second set of data pairs.

4.   (Previously presented) The high performance network address processor of claim 2

wherein a value representing a position of a selected element in the single row of a first set of

data pairs is a first input to the second pipelined lookup table, the input used to select one of the

plurality of rows of the second set of data pairs, a second input into the second pipelined lookup

table is used to locate one of the data pairs of the one of the plurality of rows.

5.   (Currently Amended) A high performance network address processor integrated circuit,

wherein the network address processor integrated circuit comprises:

        a longest prefix match lookup table engine for receiving a network address request

having a designated network destination address, the longest prefix match lookup table engine

having a plurality of pipelined lookup tables<u>, a first pipelined lookup table having a single row of</u>

a first set of data pairs, the first set of data pairs including a key value and a mask value, the

mask value indicating a number of least significant bits that are ignored within the key value, the

first set of data pairs being ordered according to corresponding mask values, and a second

pipelined lookup table having a plurality of rows of a second set of data pairs, the second set of

data pairs including a key value and a mask value, the mask value of the second set indicating a

number of least significant bits that are ignored within the key value; and

an associated data engine coupled to the longest prefix match lookup table that is capable

of receiving a key value and an output address pointer from the longest prefix match lookup table

and that is capable of providing a network address processor data output corresponding to the

designated network address pointer, the associated data engine having a first lookup table having

a plurality of rows, wherein a portion of bits of the key value is used to select one of the plurality

of rows as an output, a remaining portion of the bits of the key value identifying a row in a

second lookup table having a plurality of rows.

6.   (Currently amended) The high performance network address processor of claim 5

wherein the longest prefix match lookup engine a third pipelined lookup table having a plurality

of rows of a third set of data tuples, pairs the data tuples including a key value, a mask value and

a pointer value.

7.   (Previously presented) The high performance network address processor of claim 5

wherein a value representing a position of a selected element in the single row of a first set of

data pairs is an input to the second pipelined lookup table, the input used to select one of the

plurality of rows of the second set of data pairs.

8.   (Currently Amended) A high performance network addressing method comprising:

        providing a longest prefix match lookup engine with a network address data request and a

destination network address, wherein the longest prefix match lookup engine comprises a set of

at least two lookup tables, each of the set of at least two lookup tables including data pairs

including a corresponding key value and a corresponding mask, the corresponding mask value

indicating a number of least significant bits that are ignored within the corresponding key value,

the data pairs being ordered in each lookup table according to corresponding masks;

        searching the set of lookup tables to select a look up engine address output from the set of

lookup tables, the successive searching including,

        selecting a position within a row of a first lookup table;

        identifying a value associated with the position;

        utilizing the value as a first input to a second lookup table;

        selecting a row of the second lookup table according to the first input;

        selecting a position within the row of the second lookup table according to a second

input; and

        accessing a value stored in the position within the row of the second lookup table;

        defining a pointer to be provided provide as input to an associated data engine; and

        searching the associated data engine to provide an associated destination address output.

9.   (Currently Amended) The high performance network addressing method of claim 8 wherein successively searching the set of lookup tables comprises the smallest entry that is greater than or equal to an input search key, includes,

selecting the smallest entry that equals the input search key with a corresponding number of mask bits,

wherein if one or more entries comprise a same key, a key having a smallest mask is selected, and

wherein if no key matches, a maximum key in a row is compared with the input search key using each set of respective mask pointer pairs, each of the pointer pairs is selected to correspond to the smallest mask for which the input search key equals the maximum key in a row of a corresponding lookup table with the corresponding number of mask bits ignored.

10.   (new) The high performance network address processor of claim 1 wherein the first set of data pairs are ordered such that a pair having a lowest mask value is at an end of the single row.

11.   (new) The high performance network address processor of claim 5 wherein the first set of data pairs are ordered such that a pair having a lowest mask value is at an end of the single row.

Allowable Subject Matter

2.   Claims 1-11 are allowed.

3.   The following is an examiner's statement of reasons for allowance: Prior art fail to teach

about a longest prefix match look up table having multiple pipeline lookup tables in which each

stage of the pipeline operation is controlled by a set of data pair which include a key value and a

mask value. The mask value determines at each stage of the pipeline the least significant bits of

the key that will be ignored

        Any comments considered necessary by applicant must be submitted no later than the

payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

Allowance."

        Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Michael S. A. Delgado whose telephone number is (571) 272-

3926. The examiner can normally be reached on 7.30 AM - 5.30PM.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David A. Wiley can be reached on (571) 272-3923

        . The fax phone number for the organization where this application or proceeding is

assigned is 571-273-8300.

        Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MD

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